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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/701,090	11/04/2003	Girolamo Gallo	400.196US01	4430

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EXAMINER	
LE, DON P	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 05/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/701,090	GALLO ET AL.	
	Examiner	Art Unit	
	Don P. Le	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *21 and 22* is/are allowed.

6)☒ Claim(s) *1-3,8-10,12-14,16,23,24,29-31,35-39 and 41-48* is/are rejected.

7)☒ Claim(s) *4-7, 11, 15, 17-20, 25-28, 32-34, 40* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 4/13/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Objections

1. Claim 10 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claims 10 repeated the same elements found in claim 9.

2. Claim 41 is objected to under 37 CFR 1.75 as being a substantial duplicate of claim 35. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-3, 8-10, 12-14, 16, 23, 24, 29-31, 35-39 and 41-48 are rejected under 35 U.S.C. 102(b) as being anticipate by Michelsen (US 5,387,824).

5. With respect to claim 1, figure 2 of Michelsen discloses an output buffer, comprising:

a first stage (26, 27) and a second stage (36, 37), the first and second stages having outputs connected parallel to one another, the first stage providing buffer strength when a first stage enable signal is active, and the second stage providing buffer strength when a second stage enable signal is active.

6. With respect to claim 2, figure 2 of Michelsen discloses the first and the second stages are additive when both are enabled.

7. With respect to claims 3, 24 and 31, figure 2 of Michelsen discloses each output stage comprises:

a complementary metal oxide semiconductor (CMOS) structure having a p-channel MOS device (26) and an n-channel MOS device (27);

an AND gate (22, A NOR gate comprises an AND gate and inverted inputs) having an output connected to a gate of the n-channel transistor, and having two inputs, an input connected to a data signal and another input connected to one of a plurality of enable signals; and

an OR gate (21, a NAND gate comprises an OR gate with inverted inputs) having an output connected to a gate of the p-channel transistor, and having two inputs, an input connected to the data signal and another input connected to a complement of the one of the plurality of enable signals.

8. With respect to claim 8, figure 2 of Michelsen discloses an output buffer, comprising:

at least two parallel buffer stages (26-27, 36-37), each stage activated upon receipt of a respective stage enable signal, the stages providing a range of output buffer strengths cumulatively to a total output buffer strength.

9. With respect to claims 9 and 10, figure 2 of Michelsen discloses each output stage comprises:

a pair of CMOS components (26, 27), the first CMOS component connected to a hard coded buffer strength signal, and the second CMOS component connected to a selectable buffer strength signal; and

selection circuitry (21, 22) to select either the first CMOS component or the second CMOS component.

10. With respect to claim 12, figure 2 of Michelsen discloses an output buffer circuit, comprising:

a first output buffer stage (26, 27) for providing an output buffer strength in response to a first stage enable signal (EN1); and

at least one second output buffer stage (36, 37), wherein each second output buffer stage is adapted to selectively provide additional buffer strength in response to a respective second stage enable signal (EN2).

11. With respect to claim 13, figure 2 of Michelsen discloses each output stage comprises:

a pair of CMOS components, the first CMOS component (26) connected to a hard coded buffer strength signal, and the second CMOS component (27) connected to a selectable buffer strength signal; and

selection circuitry (21, 22) to select either the first CMOS component or the second CMOS component.

12. With respect to claim 14, figure 2 of Michelsen discloses an output buffer circuit, comprising:

a plurality of output stages (26-27, 36-37), each output stage selectable to provide a component of a total output buffer strength, each output stage comprising:

a pair of CMOS components, the first CMOS component connected to a hard coded buffer strength enable signal, and the second CMOS component connected to a selectable buffer strength enable signal; and

selection circuitry (21, 22) to select either the first CMOS component or the second CMOS component.

13. With respect to claim 16, figure 2 of Michelsen discloses an output buffer, comprising:

a first stage and a second stage, the first and second stages parallel to each other, the first stage comprising:

a first stage complementary metal oxide semiconductor (CMOS) structure having a p-channel MOS device (26) and an n-channel MOS device (27);

a first OR gate (21, NAND 21 comprise an OR gate with inverted inputs) having an output connected to a gate of the p-channel transistor, and having two inputs, an input connected to a data signal (DATA IN) and another input connected to an enable signal (EN1); and

a first AND gate (22, NOR gate 22 comprises an AND gate with inverted inputs) having an output connected to a gate of the n-channel transistor, and having two inputs, an input connected to the data signal and another input connected to the enable signal; and

the second stage comprising:

a second stage CMOS structure having a p-channel MOS device (36) and

an n-channel MOS device (37);

a second OR (31, NAND 31 comprise an OR gate with inverted inputs) gate having an output connected to a gate of the p-channel transistor, and having two inputs, an input connected to a data signal and another input connected to an enable signal; and

a second AND (32, NOR gate 32 comprises an AND gate with inverted inputs) gate having an output connected to a gate of the n-channel transistor, and having two inputs, an input connected to the data signal and another input connected to the enable signal (EN2).

14. With respect to claims 23, 29, 30 and 29, the apparatus of Michelsen is used with memory cells (see column 1, lines 5-10).

15. With respect to claims 35-39 and 41-48 the methods therein are inherent given the apparatus of Michelsen as shown in the above rejections

Allowable Subject Matter

16. Claims 21 and 22 are allowed.

17. Claims 4-7, 11, 15, 17-20, 25-28, 32-34 and 40 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

18. The following is an examiner's statement of reasons for allowance:

With respect to claims 4, 7, 11, 15, 17, 22, 25, 28 and 32, the prior art does not teach a bank of latches.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue

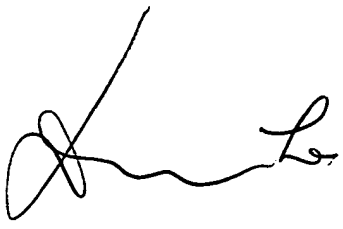
fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Don P. Le whose telephone number is 571-272-1806. The examiner can normally be reached on 7AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

4/29/2005



DON LE
PRIMARY EXAMINER